

## 1. General description

The 74HC21 is a dual 4-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- CMOS input levels
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC21D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
74HC21PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>

## 4. Functional diagram

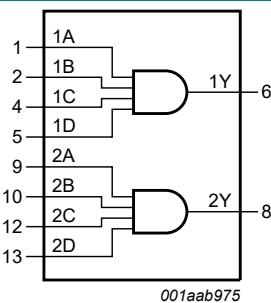


Fig. 1. Functional diagram

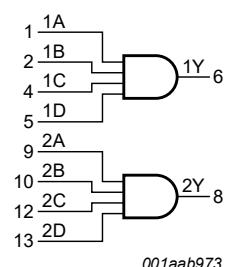


Fig. 2. Logic symbol

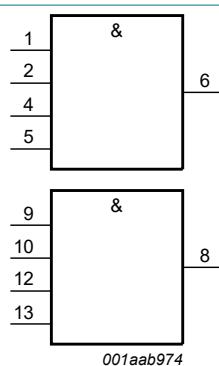


Fig. 3. IEC Logic symbol

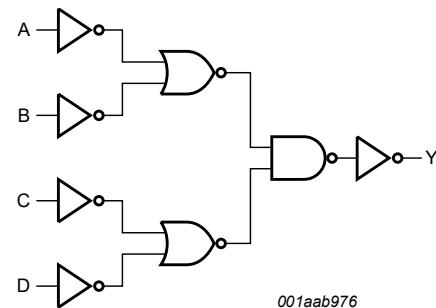
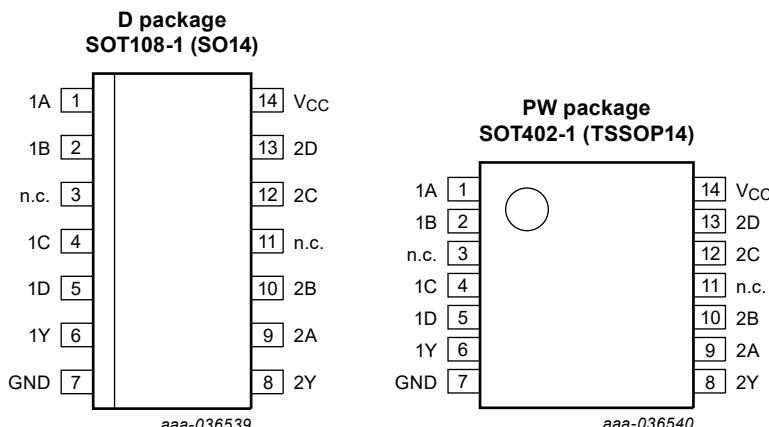


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 1B, 1C, 1D	1, 2, 4, 5	data input
n.c.	3, 11	not connected
1Y	6	data output
GND	7	ground (0 V)
2Y	8	data output
2A, 2B, 2C, 2D	9, 10, 12, 13	data input
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

Input				Output
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1]	-	±20 mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1]	-	±20 mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation		[2]	-	500 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P<sub>tot</sub> derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	$\text{pF}$

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND = 0 V; test circuit see [Fig. 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	nA, nB, nC or nD to nY; <a href="#">[1]</a> see <a href="#">Fig. 5</a>								
		$V_{CC} = 2.0$ V	-	33	110	-	140	-	165	ns
		$V_{CC} = 4.5$ V	-	12	22	-	28	-	33	ns
		$V_{CC} = 6.0$ V	-	10	19	-	24	-	28	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	10	-	-	-	-	-	ns
$t_t$	transition time	nY output; see <a href="#">Fig. 5</a> <a href="#">[2]</a>								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ <a href="#">[3]</a>	-	15	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

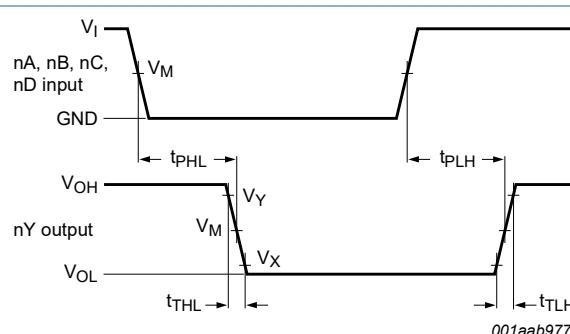
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 10.1. Waveforms and test circuit



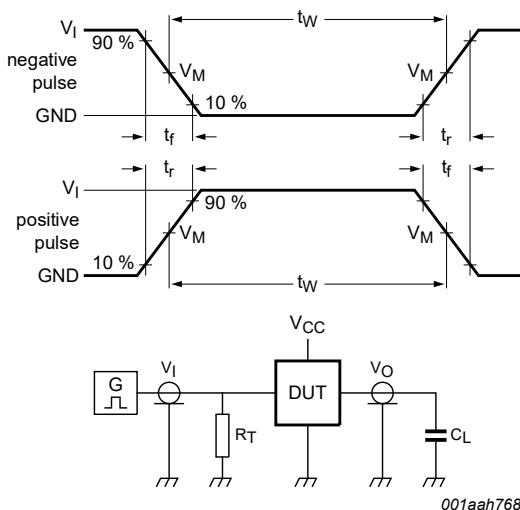
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times**

Table 8. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

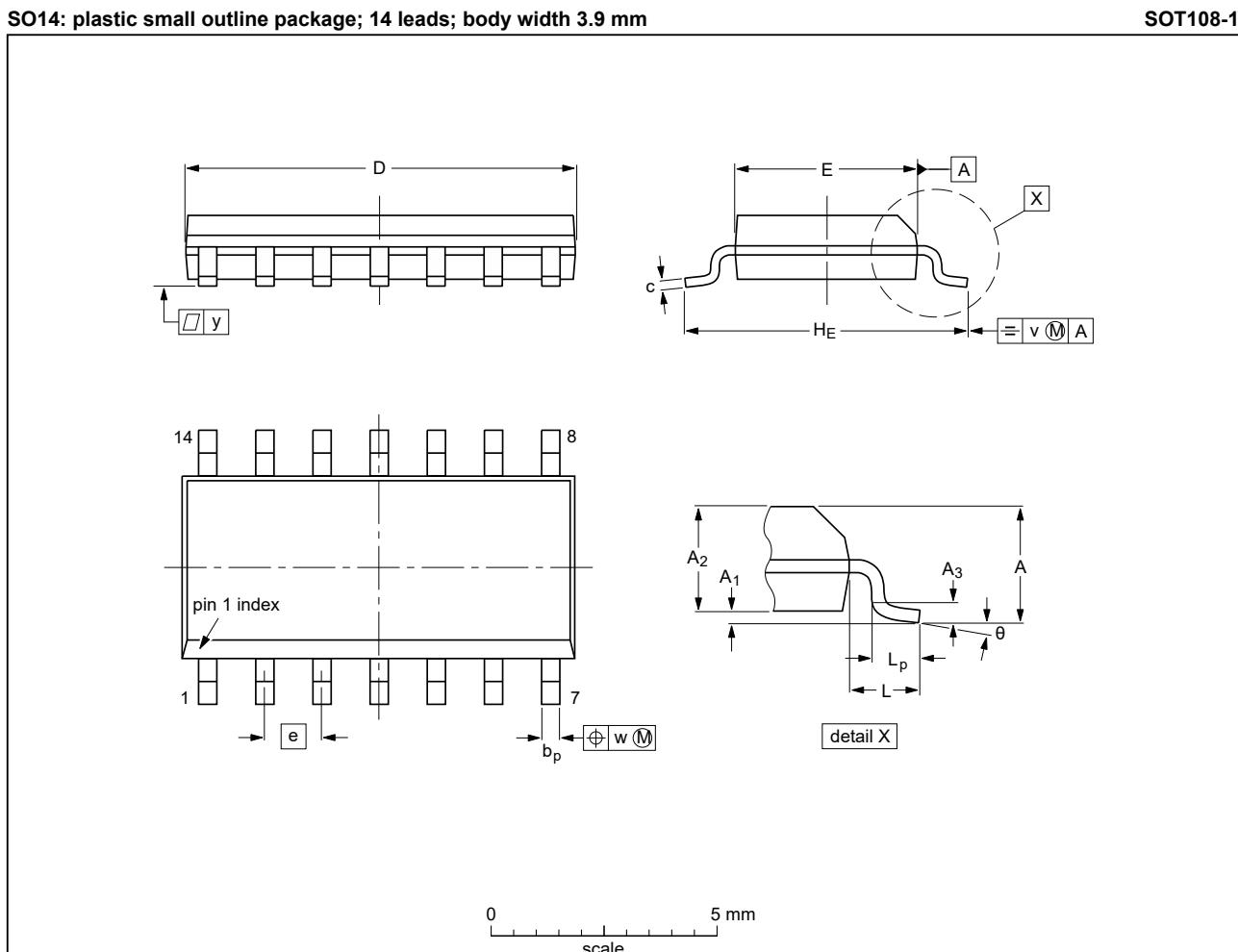
$C_L$  = load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test
$V_I$	$t_r, t_f$	$C_L$	
$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 11. Package outline



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	θ
mm	max 1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27	0.2	0.25	0.1	8°
mm	nom								1.27		1.05					
mm	min	0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max 0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
inches	nom								0.05		0.041		0.008	0.01	0.004	
inches	min	0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1\_po

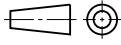
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				03-02-19 23-10-27

Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

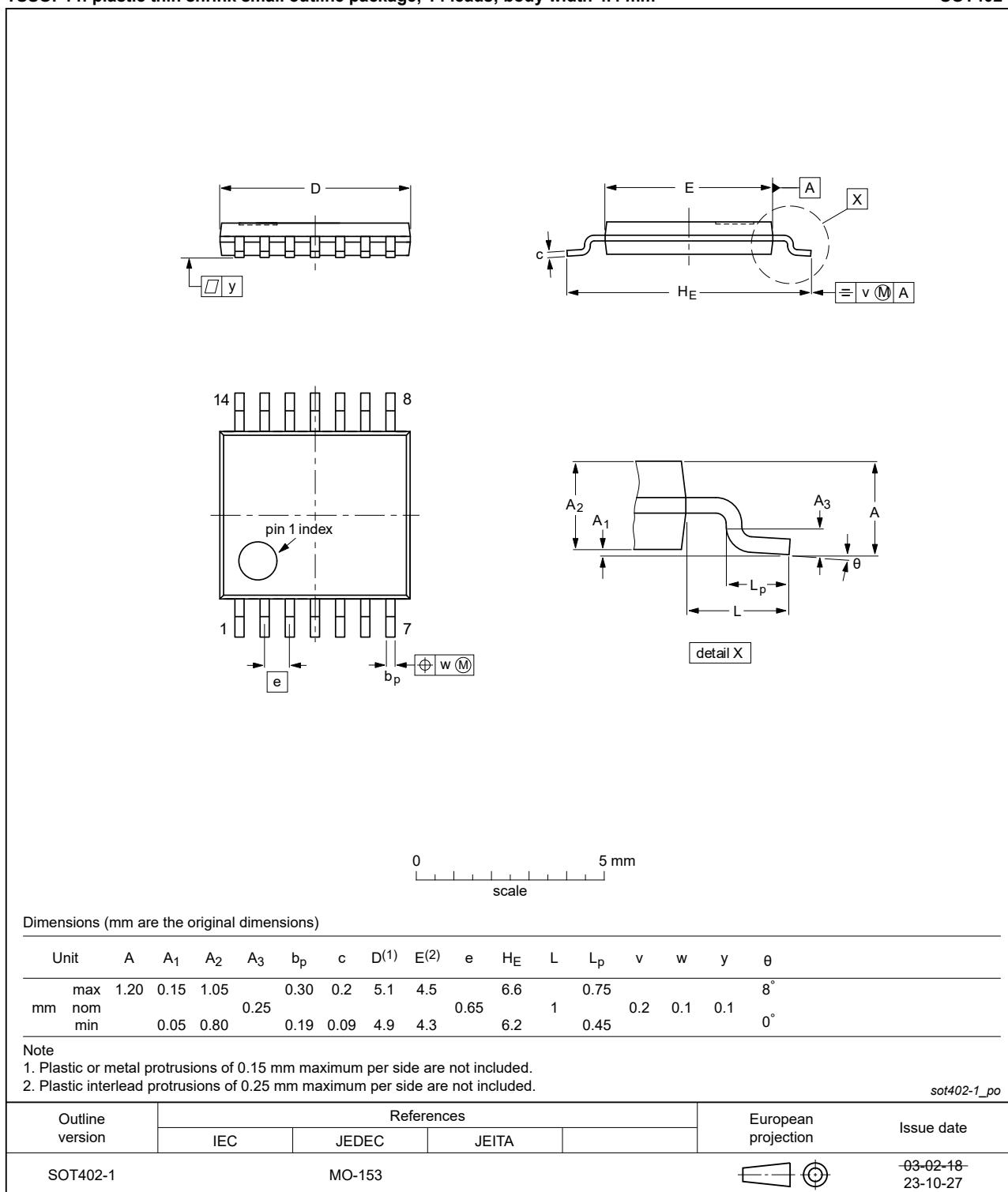


Fig. 8. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC21 v.10	20240117	Product data sheet	-	74HC21 v.9
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 7, Fig. 8</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153</li> </ul>			
74HC21 v.9	20230502	Product data sheet	-	74HC21 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC21 v.8	20210908	Product data sheet	-	74HC21 v.7
Modifications:	<ul style="list-style-type: none"> <li>Type number 74HC21DB (SOT337-1/SSOP14) removed.</li> <li><a href="#">Section 2</a> updated.</li> </ul>			
74HC21 v.7	20151130	Product data sheet	-	74HC21 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number 74HC21N (SOT27-1) removed.</li> </ul>			
74HC21 v.6	20130208	Product data sheet	-	74HC21 v.5
Modifications:	<a href="#">Section 2</a> : Typo corrected in the specified temperature range.			
74HC21 v.5	20090507	Product data sheet	-	74HC21 v.4
Modifications:	<a href="#">Table 1</a> : Type number 74HCT21PW changed to 74HC21PW.			
74HC21 v.4	20090407	Product data sheet	-	74HC21 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74HC21PW (TSSOP14 package).</li> </ul>			
74HC21 v.3	20041112	Product data sheet	-	74HC_HCT21_CNV v.2
74HC_HCT21_CNV v.2	19970828	Product specification	-	74HC_HCT21 v.1
74HC_HCT21 v.1	19901201	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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## Contents

<b>1. General description.....</b>	<b>1</b>
<b>2. Features and benefits.....</b>	<b>1</b>
<b>3. Ordering information.....</b>	<b>1</b>
<b>4. Functional diagram.....</b>	<b>1</b>
<b>5. Pinning information.....</b>	<b>2</b>
5.1. Pinning.....	2
5.2. Pin description.....	2
<b>6. Functional description.....</b>	<b>3</b>
<b>7. Limiting values.....</b>	<b>3</b>
<b>8. Recommended operating conditions.....</b>	<b>3</b>
<b>9. Static characteristics.....</b>	<b>4</b>
<b>10. Dynamic characteristics.....</b>	<b>5</b>
10.1. Waveforms and test circuit.....	5
<b>11. Package outline.....</b>	<b>7</b>
<b>12. Abbreviations.....</b>	<b>9</b>
<b>13. Revision history.....</b>	<b>9</b>
<b>14. Legal information.....</b>	<b>10</b>

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